MOSFETs Withstand Stress of Linear-Mode Operation

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For applications like electronic loads that require power MOSFETs to operate in their linear region, a novel transistor structure and process technology provides an extended FBSOA.

Power MOSFETs are most often used in switched-mode applications where they function as on-off switches. But in applications like electronic loads, linear regulators or Class A amplifiers, power MOSFETs must operate in their linear region. In this operating mode, the MOSFETs are subjected to high thermal stress due to the simultaneous occurrence of high drain voltage and current, resulting in high power dissipation.

When the thermo-electrical stress exceeds some critical limit, thermal hot spots occur in the silicon causing the devices to fail. To prevent such failure, MOSFETs operating in the linear region require high power dissipation capability and an extended forward-bias safe operating area (FBSOA).

A series of linear power MOSFETs developed by IXYS achieves an extended FBSOA capability by suppressing the positive feedback of electro-thermal instability. The design of these new MOSFETs features a nonuniform distribution of transistor cells, as well as cells with different threshold voltages.

Every transistor cell is designed with a ballast resistor at the source to limit its current. The parasitic bipolar junction transistor (BJT) of each cell is heavily bypassed so that it will not turn on under extreme electrical stress conditions. In addition, the thermal response of each power MOSFET is tested to assure no solder voids. The linear MOSFET's effectiveness can be demonstrated in the design of an electronic load developed for power-supply testing.

Second Breakdown

In power MOSFETs, the term "second breakdown" refers to a sudden reduction in a MOSFET's blocking-voltage capability followed by a loss of current control by MOSFET current. Although in most applications, MOSFETs are typically not subject to second breakdown. This potentially destructive

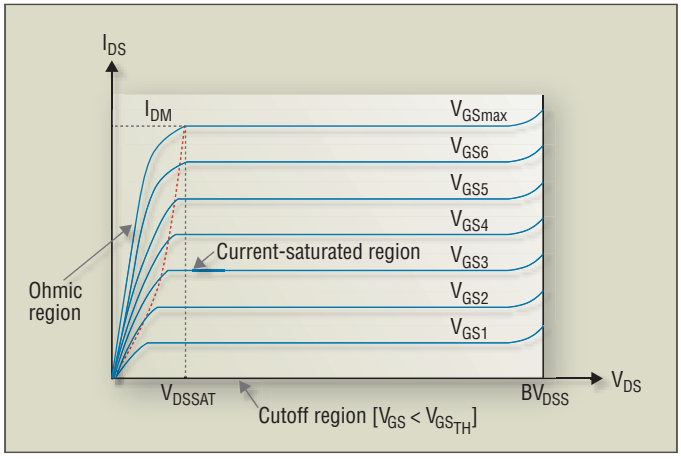

Fig. 1. *As shown in this generalized graph of output characteristics, an n-channel power MOSFET has three possible modes of operation.*

condition can occur as a result of thermal hot spots or "current focusing" in the silicon, which in turn are caused by the spurious activation of the MOSFET's parasitic BJT.

Normally, when the current attempts to self-constrict to a localized area, the increasing temperature of the spot will raise the resistance of the spot due to a positive temperature coefficient, and will redistribute the current away from the hot spot.[1] This attribute facilitates parallel operation of multiple MOSFETs.

However, applications like programmable resistors and Class A, AB amplifiers cause the power MOSFETs to operate in their linear region, where they must dissipate higher power levels than in the more common on-off switching. In such cases, the current focusing and hot spots may not be self-correcting, which can lead to device failure.

In the linear mode, a power MOSFET is subjected to high thermal stress due to the simultaneous occurrence of high drain voltage and current resulting in high power dissipation. When the thermo-electrical stress exceeds some

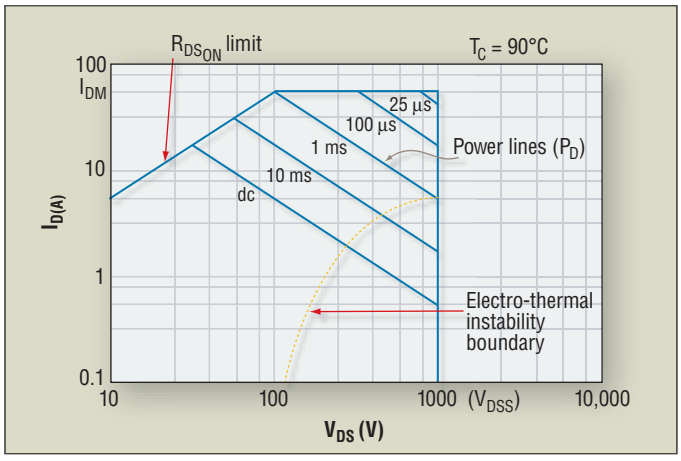

Fig. 2. *Power MOSFETs optimized for switched-mode designs have limited ability to operate in the corner of the FBSOA graph, where electro-thermal instability can occur as shown here for a typical n-channel power MOSFET.*

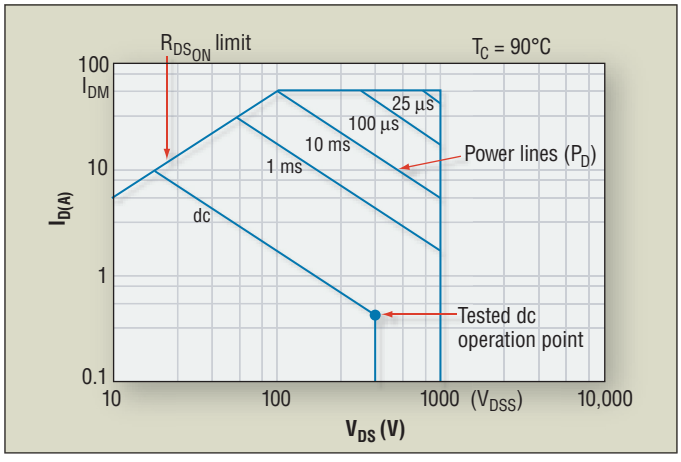

Fig. 3. *By suppressing the positive feedback of electro-thermal instability, IXYS' IXTK22N100L linear power MOSFET extends the FBSOA when compared with devices developed for switched-mode operation.*

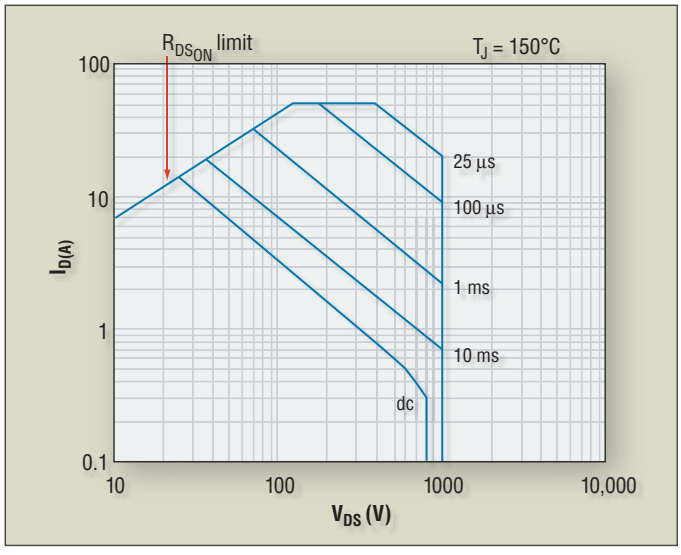

Fig. 4. *At T_C equals 90°C, the IXTK22N100L FBSOA shows its SOA point at V_{DS} equals 800 V and I_D equals 0.3 A with 240-W capability.*

critical limit, thermal hot spots occur in the silicon causing the device to fail.[2]

Fig. 1 shows a typical output characteristic of an n-channel power MOSFET in which the different modes of operation are delineated. In the cutoff region, the gate-source voltage (V_{GS}) is less than the gate-threshold voltage ($V_{GS_{TH}}$) and the device is an open circuit or off. In the ohmic region, the device acts as a resistor with an almost constant on-resistance ($R_{DS_{ON}}$) and is equal to the drain voltage (V_{DS}) divided by the drain current (I_{DS}). In the linear mode of operation, the device operates in the current-saturated region where I_{DS} is a function of the gate-source voltage (V_{GS}) and defined by:

$$I_{DS} = K(V_{GS} - V_{GS_{TH}})^2 = g_{FS}(V_{GS} - V_{GS_{TH}}), \quad \text{(Eq. 1)}$$

where K is a parameter depending on the temperature and device geometry and g_{FS} is the current gain or transconductance.

When V_{DS} is increased, the positive drain potential opposes the gate-voltage bias and reduces the surface potential in the channel. The channel inversion-layer charge decreases with increasing V_{DS} and, ultimately, becomes zero when the drain voltage equals to V_{GS} - $V_{GS_{TH}}$. This point is called the "channel pinch-off point," where the drain current becomes saturated.[3]

The FBSOA is a datasheet figure of merit that defines the maximum allowed operating points. **Fig. 2** shows a typical FBSOA characteristic for an n-channel power MOSFET. It is bound by the maximum drain-to-source voltage (V_{DSS}), maximum conduction current (I_{DM}) and constant power dissipation lines for various pulse durations.

In **Fig. 2**, the set of curves shows a dc line and four single-pulse operating lines: 10 ms, 1 ms, 100 µs and 25 µs. The top of each line is truncated to limit the maximum drain current and is bounded by a positive slope line defined by the on-resistance of the device. The right-hand side of each line is terminated at the rated drain-to-source voltage limit. Each line has a negative slope and is determined by the maximum allowed power dissipation of the device P_D:

$$P_D = \frac{(T_{J\,max} - T_C)}{Z_{\theta JC}} = V_{DS} I_D, \quad \text{(Eq. 2)}$$

where $Z_{\theta JC}$ is the junction-to-case transient thermal impedance and T_{Jmax} is the maximum allowed junction temperature of the MOSFET.

These theoretical constant power curves are derived from calculation with the assumption that junction temperature is essentially uniform across the power MOSFET die. For several reasons, this assumption is not always valid, especially for a large-die MOSFET. First, the edge of a MOSFET die soldered to the mounting tab of a power package generally has a lower temperature compared to the center of the die, which is the result of lateral heat flow. Second, material imperfections (die attach voids, thermal grease cavities, etc.) may cause a local decrease in thermal conductivity, or in other words, an increase in local temperature, with "local" meaning a specific spot on the die. Third, fluctuations in

Part No.	V_{DSS} (V)	I_D (A)	$R_{\theta JC}$ °C/W	SOA specification power (W), T_C = 90°C	Package type
IXTH24N50L	500	24	0.31	200 at V_{DS} = 400 V, I_D = 0.5 A	TO-247
IXTN46N50L	500	46	0.18	240 at V_{DS} = 400 V, I_D = 0.6 A	SOT-227B
IXTK22N100L	1000	22	0.18	240 at V_{DS} = 800 V, I_D = 0.3 A	TO-264
IXTN30N100L	1000	30	0.156	300 at V_{DS} = 600 V, I_D = 0.5 A	SOT-227B

Table 1. *Select n-channel power MOSFETs with extended FBSOA .*

dopant concentrations and gate-oxide thickness, and fixed charge will cause fluctuations of local threshold voltage and the current gain (g_{FS}) of MOSFET cells, which will also affect the local temperature of the die.

Die temperature variations are mostly harmless in the case of switched-mode operation. However, these variations can trigger catastrophic failure in linear-mode operation, with pulse durations longer than the time required for a heat transfer from the junction to the heatsink. Modern power MOSFETs optimized for switched-mode applications were found to have limited capability to operate in the bottom right-hand corner of the FBSOA graph in **Fig. 2**, the area to the right of the electro-thermal instability (ETI) boundary.

ETI can be understood as a result of a positive-feedback mechanism on the surface of a power MOSFET forced into linear mode of operation:

- There is a local increase in junction temperature
- Increasing junction temperature causes a local decrease in $V_{GS_{TH}}$, since MOSFET threshold voltage has negative temperature coefficient
- Decreasing $V_{GS_{TH}}$ causes an increase in local current density such that $J_{DS} \sim (V_{GS} - V_{GS_{TH}})^2$
- The increase in local current density causes an increase in local power dissipation, which leads to a further local increase in junction temperature.

Depending on the duration of the power pulse, heat-transfer conditions and features of the design of MOSFET cells, the ETI may cause a concentration of all the MOSFET current into a current filament and formation of a hot spot. This normally causes MOSFET cells in the affected areas to lose gate control, and turns on the parasitic BJT with consequent destruction of the device.

In response to these problems, IXYS has developed a power MOSFET structure and process that provides an extended FBSOA capability by suppressing the positive feedback of ETI. The design of these new MOSFETs features a nonuniform distribution of transistor cells, as well as cells with different threshold voltages.[3]

Die temperature variations can trigger catastropic failure in linear-mode operation.

Every transistor cell is designed with a ballast resistor at the source to limit its current.[4] The parasitic BJT of each cell is heavily bypassed so that it will not turn on under extreme electrical stress conditions. In addition, the thermal response of each power MOSFET is tested to assure no solder voids. This design has been used to develop a family of power MOSFETs with extended FBSOA suitable for reliable operation in linear mode.

Datasheets of these MOSFETs contain guaranteed FBSOA graphs. For example, **Fig. 3** shows the FBSOA graph for IXYS IXTK22N100L linear power MOSFET with its tested dc operation point marked. To illustrate the range of performance available with the linear power MOSFET design, the **table** lists key specifications for a few of the devices with extended FBSOA capability.

Based on Eq. 2, a single power MOSFET such as the IXTK22N100L with a voltage rating of 1000 V provides a power rating of 700 W. This power rating is normally used in the circuit design for switched-mode operation, but not for linear applications. For linear operation, IXYS provides a safe operating area rating that is obtained under a strict dc operation condition such as 240 W at V_{DS} equals 800 V, I_D equals 0.3 A and T_C equals 90°C for IXTK22N100L.

Application Example

Electronic loads such as those used to test power supplies can benefit from the use of linear MOSFETs with an extended FBSOA. An electronic load is essentially a programmable resistor and is typically implemented with multiple high-voltage power MOSFETs operating in parallel. In parallel operation, it's highly unlikely that current will be shared equally in each MOSFET because of variations in device geometry and mechanical assembly, which in turn cause variations in device parameters such as breakdown voltage, current gain, etc.

To assure equal current sharing, a feedback mechanism is usually employed by installing a resistor in series with each MOSFET source. That resistor monitors current in each MOSFET and develops a voltage whose value is based on the adjustment of dynamic range, the noise level at the output, the minimum load resistance and the stability of the system. It is typically designed for 1 V to 2 V maximum. The temperature stability of the system is determined by the temperature coefficient of the resistors.[2]

Consider a 2-A, 600-V regulated power supply that needs to be tested with a programmable resistor comprised of multiple power MOSFETs connected in parallel. The load needs power MOSFETs with a breakdown voltage of at least 600V and which are capable of dissipating the entire output power. The output power is defined as:

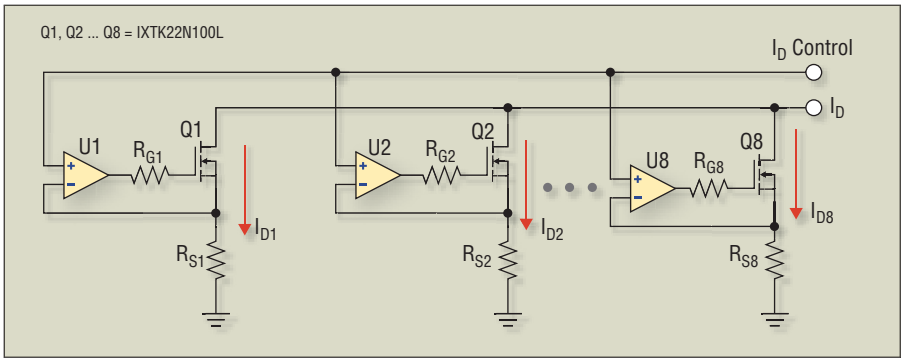

Fig. 5. *Linear MOSFETs can be used to build a programmable resistive load for testing power supplies at 2 A and 600 V.*

$$P_O = I_O \times V_O, \quad \text{(Eq. 3)}$$

where I_O equals 2 A and V_O equals 600 V. This brings the total power dissipation to: $P_O = 2 \times 600 = 1200$ W.

For this application, assume that the IXTK22N100L power MOSFET is used. This device has a voltage rating of 1000 V, a current rating of 22 A, an FBSOA (or simply SOA) rating of 240 W and a rated power dissipation of 700 W. In **Fig. 4**, the FBSOA shows its SOA point at V_{DS} equals 800 V, I_D equals 0.3 A and T_C equals 90°C with 240-W capability. Its rated power dissipation of 700 W is only applicable for switched-mode application, so for linear operation, one must use the SOA rating due to high power dissipation. Assuming a 20% safety margin with this rating, this reduces its allowable SOA rating to 192 W.

The maximum output power for the power supply is 1440 W with a 20% safety margin with the rated power rating of 1200 W. As can be seen, a single MOSFET such as IXTK22N100L cannot dissipate the total power. Thus multiple power MOSFETs connected in parallel are needed to carry the total power. The number of MOSFETs required for this application is 1440 divided by 192 equals 7.5. A typical arrangement for the programmable resistor circuit is shown in **Fig. 5**.[2]

The gate resistor shown in **Fig. 5**, connected between each op-amp output and each gate of MOSFET, is used to limit the gate current. It is optional, and its value can be chosen between 5 Ω and 50 Ω. The source resistors (RS1 through RS8) monitor the drain current in each MOSFET. The tolerance of the resistances determines the relative matching between the power MOSFETs. The voltage across the source resistor is applied to the inverting input of each op amp driving the power MOSFET and the noninverting input is connected to a control drain current that goes to the noninverting terminal of the op amp.[2]

The IXYS linear power MOSFETs overcome the limitations of conventional power MOSFETS in linear applications by extending the transistors' FBSOA. This capability has been realized by the nonuniform distribution of transistor cells and the use of cells with different threshold voltages, which helps to suppress the positive feedback of ETI. **PETech**

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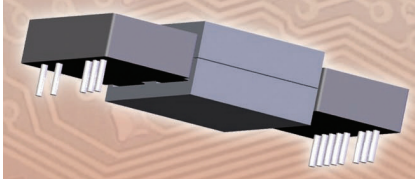

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