Zoomed out – Here you can see 4 blocks of data transfer, with the second one ending with the SCL low.

Q Saleae Logic 1.1.8 - [Connected] - [12 MHz, 100) M Samples]						
4.0 s	tart +0 ₄ 2 s +0 ₄ 3 s +	∙0 ₄ 4 s +0 ₄ 5 s +0 ₄ 6 s	5.0 s ↓ +0,1 s +0,2 s +0,3 s	+0,4 s +0,5 s +0,6 s	+0,7 s +0,8 s +0,9 s	6.0 s	Options * +0,4s +0,5s +0,6s
0 - SCL							✓ Measurements Width: 1.0204257500 s
1 - SDA					<		Period: ### Frequency: ### <u>T1</u> : ### <u>T2</u> : ###
2 - Channel 2 F 7							T1 - T2 = ### ▼ Analyzers +•
3 - Channel 3 5 7 7 ,							12C 🗴 🗖 🌩
4 - Channel 4							
5 - Channel 5							
6 - Channel 6 5							
7 - Channel 7							
•							Þ
Q >							

Zoomed in first block transfer, all looks normal – ends with an I2C stop.

Q Saleae Logic 1	1.1.8 - [Connected] - [12 MHz	z, 100 M Samples]							
100 M Samples	▼ @ 12 MHz ▼ 4206.0 ms	Start	+0.1 ms			+0.2 ms			
0 - SCL	1 _1,_								
1 - SDA	<u></u>	ę	Write [0xD0] 0x00 +	ACK Read [0xD1]	0x55 + ACK	0x32 + ACK	0x03 + ACK	0x00 + NAK	
2 - Channel 2	[<u>f, -, t,</u>]								
3 - Channel 3	<u></u>								
4 - Channel 4	(<u>f, -, t, -</u>)								
5 - Channel 5	...								
6 - Channel 6	<u></u>								
7 - Channel 7	[f,_,t,_]								
۰ ۹ >									

+0.3 ms		Detions •
	 ✓ Measurements Width: ### Period: ### Frequency: ### T1: ### T2: ### T1 - T2 = ### 	ت .
	✓ Analyzers 12C	*• X 1 2
		4

Second block, data transfer is OK, but does not end with an I2C Stop – SCL stays low for another 0.5sec.

Saleae Logic 1.1.8 - [Connected] - [12 MHz, 100 M	Samples]		
100 M Samples Image: Constraint of the second		4510700 μs 90 μs _ +10 μs +20 μs +30 μs +40 μ	45 s +50 µs +60 µs +70 µs +80 µs +90 µs
0 - SCL			
	0xD0] + ACK Read [0xD1] + A	CK 0x86 + ACK 0x32 +	ACK 0x03 + ACK 0
2 - Channel 2 🗐 🗐 🗐 🗐			
3 - Channel 3 []			
4 - Channel 4 []			
5 - Channel 5			
6 - Channel 6			
7 - Channel 7 [🗐 🚬 🚬			
Q >>			

