

Checksum: 0x17fb74b5

 Configuration Bits set in code.

Address	Value	Field	Category	Setting
1FC0_2FF0	FFFFFFFF	USERID		
		FRRSSEL	SRS Select	SRS Priority 7
		FMIIEN	Ethernet RMII/MII Enable	MII Enabled
		FETHIO	Ethernet I/O Pin Select	Default Ethernet I/O
		FCANIO	CAN I/O Pin Select	Default CAN I/O
		FUSBIDIO	USB USID Selection	Controlled by the USB Module
		FVBUSONIO	USB VBUS ON Selection	Controlled by USB Module
1FC0_2FF4	FFF879D9	FPLLIDIV	PLL Input Divider	2x Divider
		FPLLMUL	PLL Multiplier	20x Multiplier
		UPLLIDIV	USB PLL Input Divider	2x Divider
		UPLLEN	USB PLL Enable	Enabled
		FPLLODIV	System PLL Output Clock Divider	PLL Divide by 1
1FC0_2FF8	FF600DB	FNOSC	Oscillator Selection Bits	Primary Osc w/PLL (XT+,HS+,EC+PLL)
		FSOSCEN	Secondary Oscillator Enable	Disabled
		IESO	Internal/External Switch Over	Enabled
		POSCMOD	Primary Oscillator Configuration	XT osc mode
		OSCIOFNC	CLKO Output Signal Active on the OSCO Pin	Disabled
		FPBDIV	Peripheral Clock Divisor	Pb_Clk is Sys_Clk/1
		FCKSM	Clock Switching and Monitor Selection	Clock Switch Enable, FSCM Enabled
		WDTPS	Watchdog Timer Postscaler	1:1
		FWDTEN	Watchdog Timer Enable	WDT Disabled (SWDTEN Bit Controls)
1FC0_2FFC	7FFFFFFF	DEBUG	Background Debugger Enable	Debugger is disabled
		ICESEL	ICE/ICD Comm Channel Select	ICE EMUC2/EMUD2 pins shared with PGC2/PGD2
		PWP	Program Flash Write Protect	Disable
		BWP	Boot Flash Write Protect bit	Protection Disabled
		CP	Code Protect	Protection Disabled